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			WILSON, SCOTT R	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)			
	10/549,784	ELPELT ET AL.			
Office Action Summary	Examiner	Art Unit			
	SCOTT R. WILSON	2826			
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence address			
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA  - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication.  - If NO period for reply is specified above, the maximum statutory period w  - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tim vill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	l. lely filed the mailing date of this communication. (35 U.S.C. § 133).			
Status					
Responsive to communication(s) filed on 10 Ju     This action is <b>FINAL</b> . 2b) ☑ This     Since this application is in condition for allowar closed in accordance with the practice under E	action is non-final. nce except for formal matters, pro				
Disposition of Claims					
4) ☐ Claim(s) 19-38 is/are pending in the application 4a) Of the above claim(s) is/are withdraw 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 19-24,27-30,32-35,37 and 38 is/are reference of the compact of	vn from consideration.  ejected. r election requirement.  r. ☑ accepted or b)☐ objected to bedrawing(s) be held in abeyance. See	2 37 CFR 1.85(a).			
Replacement drawing sheet(s) including the correcti  11) The oath or declaration is objected to by the Ex		· <i>'</i>			
Priority under 35 U.S.C. § 119					
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  a) All b) Some * c) None of:  1. Certified copies of the priority documents have been received.  2. Certified copies of the priority documents have been received in Application No  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  * See the attached detailed Office action for a list of the certified copies not received.					
Attachment(s)  1) Notice of References Cited (PTO-892)  2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 9/19/2005.	4)  Interview Summary Paper No(s)/Mail Da 5)  Notice of Informal P 6)  Other:	te			

## **DETAILED ACTION**

## Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 19-24, 32-35, 37 and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Ueno (US 6,117,735 A). As to claim 19, Ueno, Figure 13, discloses (col. 1, lines 36-62) a semiconductor configuration for controlling a current, comprising: a) a semiconductor region (20) of a first conductivity type b) an island region (15) of a second conductivity type, opposite said first conductivity type, at least partially buried within the said semiconductor region c) a current path, between regions (13) and (14), running at least partially within said semiconductor region d) a channel region d1) forming a part of said semiconductor region, d2) having a basic doping, and d3) including at least one depletion zone (col. 1, line 49) for influencing the current; d4) said channel region including a channel conduction region (13) or (14) configured for carrying the current, said channel conduction region having the first conductivity type and a higher doping than the basic doping.

As to claim 20, Ueno, Figure 13, discloses that the current path has a vertical component.

As to claim 21, Ueno, Figure 13, discloses that the channel region, in the substrate layer (20) between regions (13) and (14), is formed as a lateral channel region.

As to claim 22, Ueno, Figure 13, (col. 1, lines 37-38) discloses the device formed as a FET.

As to claim 23, Ueno, Figure 13, (col. 1, lines 37-38) discloses the device formed as a JFET, which is a subset of a FET.

As to claim 24, Ueno, Figure 13, (col. 1, line 30) discloses that the semiconductor region is formed of silicon carbide.

As to claim 32, Ueno discloses (col. 3, lines 62-65) that the channel region is formed in an epitaxial layer.

As to claim 33, Ueno, Figure 13, discloses that the doping of the epitaxial layer is equal to the basic doping.

As to claim 34, Ueno, Figure 6, discloses that two epitaxial layers (80) and (71b), of substantially identical doping, may be formed in place of Ueno, Figure 13, layer (20).

As to claim 35, Ueno, figure 13, discloses that said semiconductor region is disposed on a substrate (10) of a second conductivity type, opposite said first conductivity type, and said current path may run through said substrate.

As to claim 37, Ueno discloses a method for producing the semiconductor configuration according to claim 19, and shown in Figure 13, the method which comprises the following method steps: providing a semiconductor substrate (10); forming an epitaxial layer (20) with a basic doping on the semiconductor substrate, the epitaxial layer including a channel region, within which a current can be influenced, via island 15); and implanting a channel conduction region (13) or (14) for carrying current into the epitaxial layer at least in a region of the channel region, the channel conduction region having a higher doping (n+) compared with the basic doping (n).

As to claim 38, Ueno, Figure 6, discloses that, when formed in the configuration of Figure 13, the epitaxial layer (80) may be a first epitaxial layer, and the method may further comprise forming a second epitaxial layer (71b), having a doping substantially identical to the basic doping, on the semiconductor substrate, the second epitaxial layer (71b) being disposed between the semiconductor substrate and the first epitaxial layer (80), and wherein the first and second epitaxial layers are applied to the semiconductor substrate progressively and one above the other.

## Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno in view of Teng et al. (US 7,145,191 B1). As to claim 27, Ueno, Figure 13, discloses the device of claim 19, as described above. Ueno does not disclose expressly at least one channel compensation region formed in said channel conduction region. Teng et al., Figure 9a, discloses a FET in which the channel conduction region (64) comprises a channel compensation region (100) or (102). At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the channel compensation regions (100) or (102) in the channel conduction region of Ueno. The motivation for doing so would have been reduce punchthrough effects (Teng et al., col. 3, lines 50-53). Therefore, it would have been obvious to combine Teng et al. with Ueno to obtain the invention as specified in claim 27.

As to claim 28, Teng et al., Figure 9a, discloses that the channel compensation region (100) or (102) has a second conductivity type, embodied as p-type, opposite what would be the first conductivity type when combined with Ueno, Figure 13, n-type. The halo regions (100) or (102) of Teng et al. may be formed adjacent the n-type regions of Ueno.

As to claim 29, Teng et al., Figure 9a, discloses that the channel compensation region (100) or (102) may have a higher dopant concentration than the channel conduction region (64).

As to claim 30, Teng et al., Figure 9a, discloses that the total charge of said first conductivity type introduced into said channel conduction region, which may be embodied as n+ lightly-doped drain regions (60E) or (62E), is approximately equal in magnitude to a total charge of said second conductivity type, p+, introduced into said channel compensation region (100) or (102).

## Allowable Subject Matter

Claims 25 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed device with specific teachings drawn to the physical

dimensions and relative doping levels which would limit the percentage of total charge between the channel conduction region and the channel region.

Claim 31 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed device with specific teachings drawn to the physical dimensions and relative doping levels which would limit the percentage of total charge between the plurality of the channel compensation regions summed together and the channel conduction region.

Claim 36 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed device with a shielding region of the first conductivity type disposed between the island region and the semiconductor region facing the substrate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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November 13, 2008

/Evan Pert/

Primary Examiner, Art Unit 2826